IN THE SPECIFICATION

The paragraph beginning at page 1, line 7 is amended as follows:

C1

This application is related to the following co-pending, commonly assigned U.S. patent applications: "DRAM Cells with Repressed Memory Metal Oxide Tunnel Insulators," ~~attorney docket no. 1303.019US1,~~ serial number 09/945,395, "Flash Memory with Low Tunnel Barrier Interpoly Insulators," ~~attorney docket no. 1303.014US1,~~ serial number 09/945,507, "Dynamic Electrically Alterable Programmable Memory with Insulating Metal Oxide Interpoly Insulators," ~~attorney docket no. 1303.024US1,~~ serial number 09/945,498, and "Field Programmable Logic Arrays with Metal Oxide and/or Low Tunnel Barrier Interpoly Insulators," ~~attorney docket no. 1303.027US1,~~ serial number 09/945,512, "SRAM Cells with Repressed Floating Gate Memory, Metal Oxide Tunnel Interpoly Insulators," ~~attorney docket no. 1303.028US1,~~ serial number 09/945,554, "Programmable Memory Address and Decode Devices with Low Tunnel Barrier Interpoly Insulators," ~~attorney docket no. 1303.029US1,~~ serial number 09/945,500, of which disclosures are herein incorporated by reference.

The paragraph beginning at page 2, line 6 is amended as follows:

C2

The original EEPROM or EARPROM and flash memory devices described by Toshiba in 1984 used the interpoly dielectric insulator for erase. ~~(See generally, F. Masuoka et al., "A new flash EEPROM cell using triple polysilicon technology," IEEE Int. Electron Devices Meeting, San Francisco, pp. 464-67, 1984; F. Masuoka et al., "256K flash EEPROM using triple polysilicon technology," IEEE Solid-State Circuits Conf., Philadelphia, pp. 168-169, 1985).~~ Various combinations of silicon oxide and silicon nitride were tried. ~~(See generally, S. Mori et al., "reliable CVD inter-poly dialectics for advanced E&EEPROM," Symp. On VLSI Technology, Kobe, Japan, pp. 16-17, 1985).~~ However, the rough top surface of the polysilicon floating gate resulted in, poor quality interpoly oxides, sharp points, localized high electric fields, premature breakdown and reliability problems.

The paragraph beginning at page 2, line 17 is amended as follows:

C3

Widespread use of flash memories did not occur until the introduction of the ETOX cell by INTEL in 1988. ~~(See generally, US PATENT 4,780,424, "Process for fabricating electrically~~

~~alterable floating gate memory devices," 25 Oct. 1988; B. Dipert and L. Hebert, "Flash memory goes mainstream," IEEE Spectrum, pp. 48-51, October, 1993; R. D. Pashley and S. K. Lai, "Flash memories, the best of two worlds," IEEE Spectrum, pp. 30-33, December 1989).~~ This extremely simple cell and device structure resulted in high densities, high yield in production and low cost. This enabled the widespread use and application of flash memories anywhere a non-volatile memory function is required. However, in order to enable a reasonable write speed the ETOX cell uses channel hot electron injection, the erase operation which can be slower is achieved by Fowler-Nordhiem tunneling from the floating gate to the source. The large barriers to electron tunneling or hot electron injection presented by the silicon oxide-silicon interface, 3.2 eV, result in slow write and erase speeds even at very high electric fields. The combination of very high electric fields and damage by hot electron collisions in the oxide result in a number of operational problems like soft erase error, reliability problems of premature oxide breakdown and a limited number of cycles of write and erase.

At page 4 line 28, please add the following:

REFERENCES

F. Masuoka et al., "A New Flash EEPROM Cell Using Triple Polysilicon Technology," IEEE Int. Electron Devices Meeting, San Francisco, pp. 464-67, 1984;

F. Masuoka et al., "256K Flash EEPROM Using Triple Polysilicon Technology," IEEE Solid-State Circuits Conf., Philadelphia, pp. 168-169, 1985;

S. Mori et al., "Reliable CVD Inter-Poly Dialectics For Advanced E&EEPROM," Symp. On VLSI Technology, Kobe, Japan, pp. 16-17, 1985;

US Patent 4,780, 424, "Process for Fabricating Electrically Alterable Floating Gate Memory Devices;"

B. Dipert and L. Hebert, "Flash Memory Goes Mainstream," IEEE Spectrum, pp. 48-51, October, 1993;

R. D. Pashley and S. K. Lai, "Flash Memories, The Best Of Two Worlds," IEEE Spectrum, pp. 30-33, December 1989;

US Patent 5,801,401, "Flash Memory With Microcrystalline Silicon Carbide As The Floating Gate Structure;"

C4

US Patent 5,852,306, "Flash Memory With Nanocrystalline Silicon Film As The Floating Gate;"

US Application Serial No. 08/908098, "Dynamic Random Access Memory Operation of a Flash Memory Device With Charge Storage On a Low Electron Affinity GaN or GaAlN Floating Gate;"

US Application Serial No. 08/903452, "Variable Electron Affinity Diamond-Like Compounds for Gates in Silicon CMOS Memories and Imaging Devices;"

US Patent.5,981,350, "Dram Cells With A Structure Surface Using A Self Structured Mask;"

US Patent 6,025, 627, "Atomic Layer Epitaxy Gate Insulators and Textured Surfaces for Low Voltage Flash Memories;"

US Application Serial No. 08/903453, "Gate Insulator For Silicon Integrated Circuit Technology by the Carburization of Silicon;"

US Application Serial No. 09/945514, "Graded Composition Gate Insulators to Reduce Tunneling Barriers In Flash Memory Devices;"

US Patent 5,691,230, "Technique for Producing Small Islands of Silicon on Insulator;"

US Application Serial No. 09/780169, "Flash Memory with Ultrathin Vertical Body Transistors;"

S. R. Pollack and C. E. Morris, "Tunneling Through Gaseous Oxidized Films of Al_2O_3," Trans. AIME, Vol. 233, p. 497, 1965;

T. P. Ma et al., "Tunneling Leakage Current In Ultrathin (< 4 nm) Nitride/Oxide Stack Dielectrics," IEEE Electron Device Letters, vol. 19, no. 10, pp. 388-390, 1998;

O. Kubaschewski and B. E. Hopkins, "Oxidation of Metals and Alloys", Butterworth, London, pp. 53-64, 1962;

K.-H. Gundlach and J. Holzl, "Logarithmic Conductivity of Al-Al_2O_3-Al Tunneling Junctions Produced by Plasma- and by Thermal-Oxidation," Surface Science, Vol. 27, pp. 125-141, 1971;

S.P.S. Arya and H.P. Singh, "Conduction Properties of Thin Al_2O_3 Films," Thin Solid Films, Vol. 91, No. 4, pp. 363-374, May 1982;

S.M. Sze, "Physics of Semiconductor Devices," 2nd Edition, Wiley-Interscience, N.Y., pp. 553-556, 1981;

C4

J. Robertson et al., "Schottky Barrier Heights of Tantalum Oxide, Barium Strontium Titanate, Lead Titanate and Strontium Bismuth Tantalate," App. Phys. Lett., Vol. 74, No. 8, pp. 1168-1170, Feb. 1999;

J. Robertson, "Band offsets of Wide-Band-Gap Oxides and Implications for Future Electronic Devices," J. Vac. Sci. Technol. B, Vol. 18, No. 3, pp. 1785-1791, 2000;

H.-S. Kim et al., "Leakage Current and Electrical Breakdown in Metal-Organic Chemical Vapor Deposited TiO_2 Dielectrics on Silicon Substrates," Appl. Phys. Lett., Vol. 69, No. 25, pp. 3860-3862, 1996;

J. Yan et al., "Structure and Electrical Characterization of TiO_2 Grown From Titanium Tetrakis-Isoproxide (TTIP) and TTIP/H_2O Ambient," J. Vac. Sci. Technol. B, Vol. 14, No. 3, pp. 1706-1711, 1966;

R.A. Swalin, "Thermodynamics of Solids, 2nd Ed." chap. 8, pp. 165-180, John Wiley and Sons, 1972;

J.M. Eldridge and J. Matisoo, "Meas. of Tunnel Current Density in a Metal-Oxide-Metal System as a Function of Oxide Thickness," Proc. 12th Intern. Conf. on Low Temperature Physics, pp. 427-428, 1971;

J.H. Greiner, "Oxidation of Lead Films by RF Sputter Etching in an Oxygen Plasma," J. Appl. Phys., Vol. 45, No. 1, pp. 32-37, 1974;

G. Simmons and A. El-Badry, "Generalized Formula For The Electric Tunnel Effect Between Similar Electrodes Separated By A Thin Insulating Film," J. Appl. Phys., Vol. 34, p. 1793, 1963; S. R. Pollack and C. E. Morris, "Tunneling Through Gaseous Oxidized Films of Al_2O_3," Trans. AIME, Vol. 233, p. 497, 1965;

Z. Hurych, "Influence of Nonuniform Thickness of Dielectric Layers on Capacitance and Tunnel Currents," Solid-State Electronics, Vol. 9, p. 967, 1966;

J. Grimblot and J. M. Eldridge, "I. Interaction of Al Films with O_2 at Low Pressures," J. Electro. Chem. Soc., Vol. 129, No. 10, pp. 2366-2368, 1982;

Grimblot and J. M. Eldridge, "II. Oxidation of Al Films," J. Electro. Chem. Soc., Vol. 129, No. 10, pp. 2369-2372, 1982;

H. Itokawa et al., "Determination Of Bandgap and Energy Band Alignment for High-Dielectric-Constant Gate Insulators Using High-Resolution X-Ray Photoelectron Spectroscopy," Ext. Abstracts Int. Conf. On Solid State Devices and Materials, pp. 158-159, 1999;

H.F. Luan, et al., "High Quality Ta_2O_5 Gate Dielectrics with $T_{ox,eq}$<10 Å," International Electron Devices Meeting Technical Digest, p. 141-144, 1999;

J. Robertson and C.W. Chen, "Schottky Barrier Heights of Tantalum Oxide, Barium Strontium Titanate, Lead Titanate, and Strontium Bismuth Tantalate," Appl. Phys. Lett., vol. 74, no. 8, pp. 1168-1170, 22 Feb. 1999;

Xin Guo, et al., "High Quality Ultra-Thin (1.5 nm) TiO_2/Si_3N_4 Gate Dielectric for Deep Submicron CMOS Technology", International Electron Devices Meeting Technical Digest, p. 137-140, 1999;

Hyeon-Seag Kim, et al., "Leakage Current and Electrical Breakdown in Metal-Organic Chemical Vapor Deposited TiO_2 Dielectrics on Silicon Substrates," vol. 69, no. 25, pp. 3860-62, 16 December, 1996;

J. Yan, et al., "Structure and Electrical Characterization of TiO_2 Grown from Titanium Tetrakis-Isoproxide (TTIP) and TTIP/H_2O Ambient," J. Vac. Sci. Technol., vol. B14, no. 3, 1706-11, 1996;

Wen-Jie Qi, et al., "MOSCAP and MOSFET Characteristics Using ZrO_2 Gate Dielectric Deposited Directly on Si," Technical Digest of 1999 IEDM, P. 145-148;

Y. Ma, et al., "Zirconium Oxide Band Gate Dielectrics with Equivalent Oxide and Thickness of Less Than 1.0 nm and Performance of Sub-micron MOSFET using a Nitride Gate Replacement Process," Digest of 1999 IEDM, p. 149-152.

Afanas' ev et al., "Electron Energy Brriers Between (100) Si and Ultrathin Stacks of SiO_2, Al_2O_3, and ZrO_2 Insulators," Appl. Phys. Lett., vol. 78, no. 20, pp. 3073-75, 2001),

K. Kukli et al., "Development of Dielectric Properties of Niobium Oxide, Tantalum Oxide, and Aluminum Oxide Based Nanolayered Materials," J. Electrochem. Soc., vol. 148, no. 2, pp. F35-F41, 2001;

Kwo, et al., "Properties of High K Gate Dielectrics Gd_2O_3 and Y_2O_3 for Si," J. Appl. Phys., vol. 89, no. 7, pp. 3920-27, 2001;

C4

Application Serial No. 09/945,507, "Flash Memory Devices With Metal Oxide Interpoly Insulators;"

J. M. Greiner, "Josephson Tunneling Barriers By RF Sputter Etching in an Oxygen Plasma," J. Appl. Phys., Vol. 42, No. 12, pp. 5151-5155, 1971;

U.S. Pat. 4,412,902, "Method of Fabrication of Josephson Tunnel Junctions;"

H. F. Luan et al., "High quality Ta_2O_5 gate dielectrics with $T_{ox,eq}$ <10 Angstroms," IEDM Tech. Digest, pp. 141-144, 1999).

Patent Application Serial No. 09/651380, "Thin Dielectric Films for DRAM Storage Capacitors;"

Application Serial No. 09/945507, "Flash Memory Devices With Metal Oxide Interpoly Insulators;"

U.S. Pat. 5,350,738, "Method of Manufacturing an Oxide Superconducting Film;"

US Application Serial No. 09/945137, "Low Cost Processes for Producing High Quality Perovskite Dielectric Films."

Page 7, lines 1-15 are amended as follows:

C5

~~Figure 9 is a table which provides relevant data on the barrier heights, energy gaps, dielectric constants and electron affinities of a wide variety of metal oxides that could be used as asymmetric tunnel barriers according to the teachings of the present invention.~~

~~Figure 10 is a table which illustrates that there are many stable, crystalline metal oxides whose compositions can vary over at least small compositional ranges.~~

~~Figure 11 is a table which illustrates that work function values can vary considerably, depending on the metal and measurement method.~~

Figure [[12]] 9 illustrates a hypothetical metal-oxide (M-O) phase diagram according to the teachings of the present invention.

Figures [[13A-13C]] 10A-10C illustrate the compositional profiles for the asymmetrical low tunnel barrier intergate insulators according to the teachings of the present invention.

Figure [[14]] 11 illustrates a block diagram of an embodiment of an electronic system according to the teachings of the present invention.

The paragraph beginning at page 19, line 18 is amended as follows:

C6

As shown in Figure 7B, the electric field is determined by the total voltage difference across the structure, the ratio of the capacitances (see Figure 7A), and the thickness (t_{ig}) of the asymmetrical interpoly dielectric 707.

$$t_{ig} = \frac{\epsilon_2 \, tox}{\epsilon_1}$$

The voltage across the asymmetrical interpoly dielectric 707 will be, $\Delta V2 = V\ C1/(C1 + C2)$, where V is the total applied voltage. The capacitances, C, of the structures depends on the dielectric constant, ϵ_r, the permittivity of free space, ϵ_o, and the thickness of the insulating layers, t, and area, A, such that $C = \epsilon_r \epsilon_o\ A/t$, Farads/cm^2, where ϵ_r is the low frequency dielectric constant. The electric field across the asymmetrical interpoly dielectric insulator 707, having capacitance, C2, will then be $E2 = \Delta V2/t2$, where t2 is the thickness of this layer.

The paragraph beginning at page 20, line 1 is amended as follows:

C7

The tunneling current in erasing charge from the floating gate 705 by tunneling to the control gate 713 will then be as shown in Figure 7B given by an equation of the form:

$$J = B \exp(- Eo/E)$$

$$J = \frac{q^2 E^2}{4\pi h \Phi} e^{-E_o/E} \qquad E_o = \frac{8\pi}{3} \frac{\sqrt{2m}\, q \Phi^{3/2}}{h}$$

where E is the electric field across the interpoly dielectric insulator 707 and Eo depends on the barrier height. Practical values of current densities for aluminum oxide which has a current density of 1 A/cm^2 at a field of about $E = 1V/20Å = 5x10^{+6}$ V/cm are evidenced in a description by Pollack. ~~(See generally, S. R. Pollack and C. E. Morris, "Tunneling through gaseous oxidized films of Al_2O_3," Trans. AIME, Vol. 233, p. 497, 1965).~~ Practical current densities for silicon oxide transistor gate insulators which has a current density of 1 A/cm^2 at a field of about E = $2.3V/23A = 1x10^{+7}$ V/cm are evidenced in a description by T. P. Ma et al. ~~(See generally, T. P. Ma et al., "Tunneling leakage current in ultrathin (< 4 nm) nitride/oxide stack dielectrics," IEEE Electron Device Letters, vol. 19, no. 10, pp. 388-390, 1998).~~

The paragraph beginning at page 20, line 16 is amended as follows:

C8

The lower electric field in the aluminum oxide interpoly insulator 707 for the same current density reflects the lower tunneling barrier (Φ_0) 721 of approximately 2 eV, shown in Figure 7B, as opposed to the 3.2 eV tunneling barrier (Φ_0) 723 of silicon oxide 703, also illustrated in Figure 7B.

The paragraph beginning at page 21, line 23 is amended as follows:

C9

(iii) The oxide growth rate and limiting thickness will increase with oxidation temperature and oxygen pressure. The oxidation kinetics of a metal may, in some cases, depend on the crystallographic orientations of the very small grains of metal which comprise the metal film ~~(see generally, O, Kubaschewski and B. E. Hopkins, "Oxidation of Metals and Alloys", Butterworth, London, pp. 53-64, 1962).~~ If such effects are significant, the metal deposition process can be modified in order to increase its preferred orientation and subsequent oxide thickness and tunneling uniformity. To this end, use can be made of the fact that metal films strongly prefer to grow during their depositions having their lowest free energy planes parallel to the film surface. This preference varies with the crystal structure of the metal. For example, fcc metals prefer to form {111} surface plans. Metal orientation effects, if present, would be larger when only a limited fraction of the metal will be oxidized and unimportant when all or most of the metal is oxidized.

The paragraph beginning at page 22, line 15 is amended as follows:

C10

Tunnel barriers comprised of metal oxide films and having different heights at their two interfaces with the contact electrodes can be made by properly oxidizing the parent metal films. Not all oxides will exhibit asymmetrical barrier characteristics. Asymmetrical barriers can be formed on those oxides that are stable over small composition ranges so that gradients can be formed which produce different barrier heights at the top and bottom contacts. Thus SiO_2 and PbO films, made by conventional processes, are stable only at their stoichiometric compositions: hence, they can only serve as symmetrical barriers. However, there are many stable, crystalline metal oxides whose compositions can vary over at least small compositional ranges. The same is evidenced in the table shown in Figure 10 which is compiled from data in a text by Kubaschewski and Hopkins. ~~(See generally the comprehensive review by O. Kubaschewski and~~

C10

~~B.E. Hopkins, "Oxidation of Metals and Alloys," Butterworth, London (1962)).~~ As but one example of oxide stoichiometric effects, note that thermal oxidation of aluminum below ~300 degrees Celsius produces Al_2O_3 films that become less metal-rich as the oxide thickens from ~10 to 30 or 40 Angstroms. ~~(See generally, J. Grimblot and J.M. Eldridge, "II. Oxidation of Al Films," J. Electrochem. Soc., Vol. 129, No. 10, pp. 2369-2372, 1982).~~ This very small compositional variation (~10^{20} Al atoms/cm^3) leads to significant differences in barrier heights and injected currents in $Al/Al_2O_3/Al$ structures of 0.2 eV and 10X, respectively. ~~(See generally, K. H. Gundlach and J. Holzl, "Logarithmic conductivity of Al-Al_2O_3-Al tunneling junctions produced by plasma- and by thermal-oxidation," Surface Science, Vol. 27, pp. 125-141, 1971; S.P.S. Arya and H.P. Singh, "Conduction properties of thin Al_2O_3 films," Thin Solid Films, Vol. 91, No. 4, pp. 363-374, May 1982).~~ Other oxides including those containing alkaline earth and transition metal elements form variable oxide compositions and thus meet that criteria for acting as asymmetrical barriers. Most importantly and novel, it will be shown that the compositional gradients across these oxides can be uniquely controlled using certain thermodynamic characteristics of metal/oxide systems.

The paragraph beginning at page 23, line 18 is amended as follows:

C11

A second approach for forming an asymmetric barrier is to employ a control contact plate that has a different work function than that under the metal oxide dielectric layer. According to this method very asymmetric barriers can be produced by judicious selection of contact metals since their work functions can vary from low values of ~2.7 eV for rare earth metals to ~5.8 eV for platinum. ~~(See generally, S.M. Sze, "Physics of Semiconductor Devices," 2nd Edition, Wiley-Interscience, N.Y., pp. 553-556, 1981).~~ Note that the reported work function values can vary considerably, depending on the metal and measurement method. The same is evidenced in ~~the table shown in Figure 11~~ TABLE A which is compiled from data in the Handbook of Chemistry and Physics.

TABLE A

Metal	Oxygen Solub., at %	Oxide Stability Range	Semiconductor Type	Structure Temp.	Transform Temp., °C
Ta	0.8	$TaO_{4.7-5.0}$	n	Orthorhom.	t.p. 1350

Ti	28	$TiO_{3.82-5.0}$	n	Rutile	m.p. 1920
Zr	29	$ZrO_{3.66-5.0}$	n	Monoclinic	t.p. 1170
Nb	2.3	$Nb_2O_{4.86-5.0}$	n	Monoclinic	m.p. 1495
Al	v. small	$Al_2O_{2.000-3.0}$	n	Corundum	m.p. 2050
Pb	v. small	PbO	(p)	Orthorhom.	m.p. 885
Si	v.small	SiO_2	n or p	Tetra. (Cyst.)	m.p. 1713

C11

Such differences can be attributed to the effects of impurity segregation, surface oxidation, grain orientation and stress. Cesiated tungsten is a well-known example of the segregation effect: very low concentrations of cesium segregates to heated tungsten surfaces, effectively changing the work function from that of W to that of Cs. A novel method will be given below for preventing such unwanted surface segregation of impurities.

The paragraph beginning at page 24, line 5 is amended as follows:

C12

Finally, both oxide composition gradients, described in connection with ~~Figure 10~~ TABLE A, and electrode work function effects described in connection with ~~Figure 11~~ TABLE B can be utilized together to produce an even larger variety of asymmetrical tunnel junction barriers according to the teachings of the present invention.

TABLE B

Metal	Orientation	Work Function, eV
Eu	Polycryst.	2.5
Sm	Polycryst.	2.7
Y	Polycryst.	3.1
Al	(111)	4.26
Cu	(111)	4.94
Au	(111)	5.31
Ti	Polycryst.	4.33
Rh	Polycryst.	4.98
Pt	Polycryst.	5.64

C12

Zr	Polycryst.	4.05
Ta	Polycryst.	4.25
Nb	Polycryst.	4.36
Si	(100), n-type	4.91

The paragraph beginning at page 24, line 11 is amended as follows:

C13

In order to discuss the implementation of the above, it is necessary to provide more information. Thus, Figure 8 graphically illustrates the dependence of the barrier height for current injection on the work function and electron affinity of a given, homogeneous dielectric film. ~~Figure 9 is a table which~~ TABLE C provides relevant data on the barrier heights, energy gaps, dielectric constants and electron affinities of a wide variety of nominal oxide compositions that could be used as asymmetric tunnel barriers according to the teachings of the present invention.

TABLE C

	E_G	ϵ_r	$\epsilon\infty$	χ	Φ_o(Pt)	Φ_o(Al)	Φ_o(Other)
Conventional Insulators							
SiO_2	~ 8eV	4	2.25	0.9 eV		3.2 eV	4.0 (Si)
Si_3N_4	~ 5 eV	7.5	3.8	1.7		2.4 eV	
Metal Oxides							
Al_2O_3	7.6 eV	9 - 11	3.4	2.1		~ 2 eV	
NiO							
Transition Metal Oxides							
Ta_2O_5	4.6 – 4.8		4.8	3.3	2.0	0.8 eV	1.0 (Ta)
TiO_2	6.8	30-80	7.8	3.9	~ 1.2 eV		0.4 (Ti)
ZrO_2	5 – 7.8	18.5-25	4.8	2.5		1.4	2.7 (Zr)
Nb_2O_5	3.1	35-50					
Y_2O_3	6		4.4	1.8		2.3	1.3 (Y)

C13

Perovskite Oxides							
$SrBi_2Ta_2O_3$	4.1		5.3	3.3	2.0	0.8 eV	
$SrTiO_3$	3.3		6.1	3.9	1.4	0.2 eV	
$PbTiO_3$	3.4		6.25	3.5	1.8	0.6 eV	
$PbZrO_3$	3.7		4.8	3.9	~1.4	0.2 eV	

~~(See generally, H.F. Luan et al., "High quality Ta_2O_5 gate dielectrics with T_{ox} equil. 10 Angstroms," IEDM Tech. Digest, pp. 141-144, 1999; J. Robertson et al., "Schottky barrier heights of tantalum oxide, barium strontium titanate, lead titanate and strontium bismuth tantalate," App. Phys. Lett., Vol. 74, No. 8, pp. 1168-1170, Feb. 1999; J. Robertson, "Band offsets of wide-band-gap oxides and implications for future electronic devices," J. Vac. Sci. Technol. B, Vol. 18, No. 3, pp. 1785-1791, 2000; Xin Guo et al., "High quality ultra-thin (1.5 nm) TiO_2/Si_3N_4 gate dielectric for deep submicron CMOS technology," IEDM Tech. Digest, pp. 137-140, 1999; H. S. Kim et al., "Leakage current and electrical breakdown in metal-organic chemical vapor deposited TiO_2 dielectrics on silicon substrates," Appl. Phys. Lett., Vol. 69, No. 25, pp. 3860-3862, 1996; J. Yan et al., "Structure and electrical characterization of TiO_2 grown from titanium tetrakis-isoproxide (TTIP) and TTIP/H_2O ambient," J. Vac. Sci. Technol. B, Vol. 14, No. 3, pp. 1706-1711, 1966).~~

The paragraph beginning at page 25, line 5 is amended as follows:

C14

Other properties of some simple Transition Metal oxides (TM oxides) have been shown in TABLE A ~~the table provided in Figure 10~~. Note that their compositions can vary from metal-rich to their stoichiometric values. The data given in TABLE A ~~Figure 10~~ clearly show that many of the oxides cited have a range of stable compositions around their nominal values. This, along with related, established oxidation data and theory ~~(see generally, the comprehensive review by O. Kubaschewski and B.E. Hopkins, "Oxidation of Metals and Alloys," Butterworth, London (1962))~~ and the thermodynamic properties of solid multi-component solid systems ~~(see, for example, R.A. Swalin, "Thermodynamics of Solids, 2nd Ed." chap. 8, pp. 165-180, John Wiley and Sons, 1972)~~ lead to the rigorous understanding required to uniquely and controllably

C14

form asymmetrical oxide tunnel barriers as used by the present invention. Further explanation is as follows:

The paragraph beginning at page 26, line 9 is amended as follows:

C15

(v) Notwithstanding the above, a quasi-stable equilibrium exists between the growing oxide film and the underlying, partially-oxidized metal. This quasi-equilibrium can be represented schematically by a generic phase diagram for a TM(O)/TM oxide/O_2 system, as shown in Figure 9 ~~Figure 12~~. As shown in Figure 9 ~~Figure 12~~, the development of the co-existing phases are shown at various stages of the metal film oxidation, e.g., $C_1°$, $C_2°$, and $C_3°$, respectively. For clarity, this diagram is not drawn to scale. In accord with the Phase Rule and underlying thermodynamics, Figure 9 ~~Figure 12~~ shows:

The paragraph beginning at page 28, line 3 is amended as follows:

C16

In addition to controlling compositional gradients across ultra-thin oxide insulating films, it is encouraging to note that oxide growth on most metals during low temperature oxidation can be very exactly controlled. This is a consequence of the fact that the thickness of an oxide grown on an initially clean surface is proportional to either log (oxidation time) or $\log^{-1}$ (time). It is experimentally difficult to differentiate the two time dependencies. Accordingly oxide growth is very rapid initially but drops to low or negligible values after forming a stable oxide thickness in the range of 20-50 Angstroms. Titanium, zirconium, vanadium, tantalum and aluminum, for example, all oxidize according to a logarithmic time dependence at temperatures below ~300 degrees Celsius. ~~(See generally, the comprehensive review by O. Kubaschewski and B.E. Hopkins, "Oxidation of Metals and Alloys," Butterworth, London (1962)).~~ Control of oxidation time is quite sufficient, other conditions being maintained, to achieve a thickness control well within an Angstrom of the target value. This point has been well-demonstrated in earlier studies involving various metals including lead. ~~(See generally, J.M. Eldridge and J. Matisoo, "Meas. of tunnel current density in a Metal-Oxide-Metal system as a function of oxide thickness," Proc. 12th Intern. Conf. on Low Temperature Physics, pp. 427-428, 1971; J.H. Greiner, "Oxidation of lead films by rf sputter etching in an oxygen plasma," J. Appl. Phys., Vol. 45, No. 1, pp. 32-37, 1974).~~

The paragraph beginning at page 28, line 23 is amended as follows:

C17

Figures 10A-10C ~~13A-13C~~ illustrate the compositional profiles for the asymmetrical low tunnel barrier intergate insulators according to the teachings of the present invention. Figure 10A ~~13A~~ shows the compositional profile before oxidation. Figure 10B ~~13B~~ shows the compositional profile during oxidation with the coexisting phases indicated. Figure 10C ~~13C~~ shows the compositional profile at the end of oxidation.

The paragraph beginning at page 29 line 2 is amended as follows:

C18

As stated above, the conventional large barrier insulating dielectrics are silicon oxide and silicon nitride. ~~(See generally, T.P. Ma et al., "Tunneling leakage current in ultra-thin (<4 nm) nitride/oxide stack dielectrics," IEEE Electron Device Letters, vol. 19, no. 10, pp. 388-390, 1998).~~ The realities are that silicon oxide is not an optimum choice for memory type devices, because the 3.2eV tunnel barrier is too high resulting in premature failure of the insulators and limiting the number of operational cycles to be in the order of 10^5 to 10^7.

The paragraph beginning at page 29 line 9 is amended as follows:

C19

According to one embodiment of the present invention, an asymmetrical low tunneling barrier interpoly insulator is used instead, such as Al_2O_3 with a tunneling barrier of approximately 2.0 eV. A number of studies have dealt with electron tunneling in $Al/Al_2O_3/Al$ structures where the oxide was grown by "low temperature oxidation" in either molecular or plasma oxygen. ~~(See generally, S. M. Sze, Physics of Semiconductor Devices, Wiley, NY, pp. 553-556, 1981; G. Simmons and A. El Badry, "Generalized formula for the electric tunnel effect between similar electrodes separated by a thin insulating film," J. Appl. Phys., Vol. 34, p. 1793, 1963; S. R. Pollack and C. E. Morris, "Tunneling through gaseous oxidized films of Al_2O_3," Trans. AIME, Vol. 233, p. 497, 1965; Z. Hurych, "Influence of nonuniform thickness of dielectric layers on capacitance and tunnel currents," Solid State Electronics, Vol. 9, p. 967, 1966; S. P. S. Arya and H. P. Singh, "Conduction properties of thin Al_2O_3 films," Thin Solid Films, Vol. 91, No. 4, pp. 363-374, May 1982; K. H. Gundlach and J. Holzl, "Logarithmic conductivity of Al-Al_2O_3-Al tunneling junctions produced by plasma- and by thermal-~~

C19

~~oxidation", surface Science, Vol. 27, pp. 125-141, 1971).~~ Before sketching out a processing sequence for these tunnel barriers, note:

The paragraph beginning at page 30 line 1 is amended as follows:

C20

(ii) Tunnel currents are asymmetrical in this system with somewhat larger currents flowing when electrons are injected from Al/Al_2O_3 interface developed during oxide growth. This asymmetry is due to a minor change in composition of the growing oxide: there is a small concentration of excess metal in the Al_2O_3, the concentration of which diminishes as the oxide is grown thicker. The excess Al^{+3} ions produce a space charge that lowers the tunnel barrier at the inner interface. The oxide composition at the outer Al_2O_3/Al contact is much more stoichiometric and thus has a higher tunnel barrier. *In situ* ellipsometer measurements on the thermal oxidation of A1 films deposited and oxidized *in situ* support this model ~~(see generally, J. Grimblot and J. M. Eldridge, "I. Interaction of Al films with O_2 at low pressures", J. Electro. Chem. Soc., Vol. 129, No. 10, pp. 2366-2368, 1982. J. Grimblot and J. M. Eldridge, "II. Oxidation of Al films", ibid, 2369-2372, 1982)~~. In spite of this minor complication, $Al/Al_2O_3/Al$ tunnel barriers can be formed that will produce predictable and highly controllable tunnel currents that can be ejected from either electrode. The magnitude of the currents are still primarily dominated by Al_2O_3 thickness which can be controlled via the oxidation parametrics.

The paragraph beginning at page 30 line 18 is amended as follows:

C21

With this background, the following outlines one process path out of several that can be used to form Al_2O_3 tunnel barriers. Here the aluminum is thermally oxidized although one could use other techniques such as plasma oxidation ~~(see generally, S. R. Pollack and C. E. Morris, "Tunneling through gaseous oxidized films of Al_2O_3," Trans. AIME, Vol. 233, p. 497, 1965; K. H. Gundlach and J. Holzl, "Logarithmic conductivity of Al-Al_2O_3-Al tunneling junctions produced by plasma- and by thermal- oxidation", Surface Science, Vol. 27, pp. 125-141, 1971)~~ or rf sputtering in an oxygen plasma ~~(see generally, J. H. Greiner, "Oxidation of lead films by rf sputter etching in an oxygen plasma", J. Appl. Phys., Vol. 45, No. 1, pp. 32-37, 1974)~~. For the sake of brevity, some details noted above will not be repeated.

The paragraph beginning at page 31 line 4 is amended as follows:

C22

(ii) Oxidize the aluminum *in situ* in molecular oxygen using temperatures, pressure and time to obtain the desired Al_2O_3 thickness. The thickness increases with log (time) and can be controlled via time at a fixed oxygen pressure and temperature to *within 0.10 Angstroms*, when averaged over a large number of aluminum grains that are present under the counter-electrode. One can readily change the Al_2O_3 thickness from ~15 to 35A by using appropriate oxidation parametrics ~~(e.g., see Figure 3, J. Grimblot and J. M. Eldridge, "I. Interaction of Al films with O_2 at low pressures", J. Electro. Chem. Soc., Vol. 129, No. 10, pp. 2366-2368, 1982)~~. The oxide will be amorphous and remain so until temperatures in excess of 400 degrees Celsius are reached. The initiation of recrystallization and grain growth can be suppressed, if desired, via the addition of small amounts of glass forming elements (e.g., Si) without altering the growth kinetics or barrier heights significantly.

The paragraph beginning at page 31, line 21 is amended as follows:

C23

As mentioned above, this oxide insulator is used as an asymmetrical low tunnel barriers, of the order of 2.0 eV, as the inter-poly or inter-gate dielectric insulators. The characteristics of such oxide insulators have been summarized in Figure 9. According to the teachings of the present invention, asymmetrical low barriers are utilized in programmable array logic or memory device which are easy to write and/or erase. To achieve the correct barrier height different contact metals as for instance aluminum (A1) and platinum (Pt) may be used as illustrated in Figures 2 and 3. As stated previously, very asymmetrical barriers can be produced by the judicious selecting of contact metals since their work functions can vary from low values of ~2.7 eV for rare earth metals to ~5.8 eV for platinum. That is according to the teachings of the present invention the floating gate includes a polysilicon floating gate having a metal layer formed thereon in contact with the asymmetrical low tunnel barrier intergate insulator. Additionally, as described above, the control gate includes a polysilicon control gate with a metal layer, having a work function different from that of the metal layer formed on the floating gate, formed thereon in contact with the asymmetrical low tunnel barrier intergate insulator. In conjunction with the invention, the asymmetrical low tunnel barrier interpoly insulator is formed such that the tunnel barrier is approximately 2.0 eV. It is again noted, that according to the

C23

teachings of the present invention, relatively low barrier heights, e.g. in the 0.4 to 2.7 eV range, can accrue on growing TM oxide films on TM layers. (See again the estimated values cited in the last column of ~~Figure 9~~ Table C). While these barrier heights are only estimates, they are considerably lower than that encountered in Si/SiO_2 and Al/SiO_2 barriers.

The paragraph beginning at page 32, line 19 is amended as follows:

C24

The band gap energies and barrier heights of some conventional gate insulators as silicon oxide, silicon nitride and aluminum oxide as well as tantalum oxide have been investigated and described in detail ~~(see generally, H. Itokawa et al., "Determination of bandgap and energy band alignment for high-dielectric-constant gate insulators using high-resolution x-ray photoelectron spectroscopy," Ext. Abstracts Int. Conf. On Solid State Devices and Materials, pp. 158-159, 1999)~~. Formation of single and double-layer dielectric layers of oxides of Ta_2O_5 and similar transition metal oxides can be accomplished by thermal as well as plasma oxidation of films of these metals. ~~(See generally, H.F. Luan, et al., "High quality Ta_2O_5 gate dielectrics with T_{ox} $_{eq}$<10 Å," International Electron Devices Meeting Technical digest, p. 141-144, 1999; J. Robertson and C.W. Chen, "Schottky barrier heights of tantalum oxide, barium strontium titanate, lead titanate, and strontium bismuth tantalate," Appl. Phys. Lett., vol. 74, no. 8, pp. 1168-1170, 22 Feb. 1999).~~

The paragraph beginning at page 33, line 4 is amended as follows:

C25

~~For~~ TiO_2, ZrO_2, Nb_2O_5, Gd_2O_3 and Y_2O_3 have been disclosed. ~~see generally, John Robertson, "Band offsets of wide-band-gap oxides and implications for future electronic devices," J. Vac. Sci. Technol., vol. B 18, no. 3, 1785-94, May-Jun, 2000; Xin Guo, et al., "High quality ultra-thin (1.5 nm) TiO_2/Si_3N_4 gate dielectric for deep submicron CMOS technology", International Electron Devices Meeting Technical Digest, p. 137-140, 1999; Hyeon-Seag Kim, et al., "Leakage current and electrical breakdown in metal-organic chemical-vapor-deposited TiO_2 dielectrics on silicon substrates," vol. 69, no. 25, pp. 3860-62, 16 December, 1996; J. Yan, et al., "Structure and electrical characterization of TiO_2 grown from titanium tetrakis-isoproxide (TTIP) and TTIP/H_2O ambient," J. Vac. Sci. Technol., vol. B14, no. 3, 1706-11, 1996), ZrO_2 (Wen-Jie Qi, et al., "MOSCAP and MOSFET characteristics using ZrO_2 gate dielectric deposited directly~~

C25

~~on Si," Technical Digest of 1999 IEDM, P. 145-148; Y. Ma, et al., "Zirconium Oxide Band Gate Dielectrics with Equivalent Oxide and Thickness of Less Than 1.0 nm and Performance of Sub-micron MOSFET using a Nitride Gate Replacement Process," Digest of 1999 IEDM, p. 149-152.~~

33 19

The paragraph beginning at page ~~34~~, line ~~1~~ is amended as follows:

~~See also, Afanas'ev et al., "Electron energy barriers between (100) Si and ultrathin stacks of SiO_2, Al_2O_3, and ZrO_2 insulators," Appl. Phys. Lett., vol. 78, no. 20, pp. 3073-75, 2001), Nb_2O_5 (K. Kukli et al., development of dielectric properties of niobium oxide, tantalum oxide, and aluminum oxide based nanolayered materials," J. Electrochem. Soc., vol. 148, no. 2, pp. F35-F41, 2001), Gd_2O_3 and Y_2O_3 (J. Kwo, et al., "Properties of high k gate dielectrics Gd_2O_3 and Y_2O_3 for Si," J. Appl. Phys., vol. 89, no. 7, pp. 3920-27, 2001).~~

The paragraph beginning at page 34, line 1 is amended as follows:

According to the teachings of the present invention, several of the above implementations have been described in considerable detail in a co-pending~~, co-filed~~ application by L. Forbes and J.M. Eldridge, entitled "FLASH MEMORY DEVICES WITH METAL OXIDE INTERPOLY ~~INTERPLOY~~ INSULATORS," Application Serial No. 09/945,507, filed August 30, 2001 ~~attorney docket number 1303.014us1~~. In some cases the characteristics of the resulting dielectric insulators are not yet well known or well defined. Part of this detail is recounted as follows.

C26

The paragraph beginning at page 34, line 7 is amended as follows:

C27

For example, single layers of Ta_2O_5, TiO_2, ZrO_2, Nb_2O_5 and similar transition metal oxides can be formed by "low temperature oxidation" of numerous Transition Metal (e.g., TM oxides) films in molecular and plasma oxygen and also by rf sputtering in an oxygen plasma. The thermal oxidation kinetics of these metals have been studied for decades with numerous descriptions and references to be found in the book by Kubaschewski and Hopkins ~~(see generally, O. Kubaschewski and B. E. Hopkins, "Oxidation of Metals and Alloys", Butterworth, London, pp. 53-64, 1962).~~ In essence, such metals oxidize via logarithmic kinetics to reach thicknesses of a few to several tens of angstroms in the range of 100 to 300 degrees Celsius. Excellent oxide barriers for Josephson tunnel devices can be formed by rf sputter etching these

metals in an oxygen plasma ~~(see generally, J. M. Greiner, "Josephson tunneling barriers by rf sputter etching in an oxygen plasma," J. Appl. Phys., Vol. 42, No. 12, pp. 5151-5155, 1971; O. Michikami et al., "Method of fabrication of Josephson tunnel junctions," U.S. Pat. 4,412,902, Nov. 1, 1983).~~ Such "low temperature oxidation" approaches differ considerably from MOCVD processes used to produce these TM oxides. MOCVD films require high temperature oxidation treatments to remove carbon impurities, improve oxide stoichiometry and produce recrystallization. Such high temperature treatments also cause unwanted interactions between the oxide and the underlying silicon and thus have necessitated the introduction of interfacial barrier layers. ~~(See, for example, H. F. Luan et al., "High quality Ta_2O_5 gate dielectrics with $T_{ox,eq}$ <10 Angstroms," IEDM Tech. Digest, pp. 141-144, 1999).~~

The paragraph beginning at page 35, line 1 is amended as follows:

A new approach was described in a copending application by J. M. Eldridge, entitled "Thin Dielectric Films for DRAM Storage Capacitors," patent application Serial No. 09/651,380 filed Aug. 29, 2000 that utilizes "low temperature oxidation" to form duplex layers of TM oxides. Unlike MOCVD films, the oxides are very pure and stoichiometric as formed. They do require at least a brief high temperature (est. 700 to 800 degrees Celsius but may be lower) treatment to transform their microstructures from amorphous to crystalline and thus increase their dielectric constants to the desired values (> 20 or so). Unlike MOCVD oxides, this treatment can be carried out in an inert gas atmosphere, thus lessening the possibility of inadvertently oxidizing the poly-Si floating gate. While this earlier disclosure was directed at developing methods and procedures for producing high dielectric constant films for storage cells for DRAMs, the same teachings can be applied to producing thinner asymmetrical metal oxide tunnel films for the programmable array logic and memory devices described in this disclosure. The dielectric constants of these TM oxides are substantially greater (>25 to 30 or more) than those of PbO and Al_2O_3. Duplex layers of these high dielectric constant oxide films are easily fabricated with simple tools and also provide improvement in device yields and reliability. Each oxide layer will contain some level of defects but the probability that such defects will overlap is exceedingly small. Effects of such duplex layers were first reported by J. M. Eldridge, one of the present authors, and are well known to practitioners of the art. It is worth mentioning that highly

C28

reproducible TM oxide tunnel barriers can be grown by rf sputtering in an oxygen ambient, as referenced above ~~(see generally, J. M. Greiner, "Josephson tunneling barriers by rf sputter etching in an oxygen plasma," J. Appl. Phys., Vol. 42, No. 12, pp. 5151-5155, 1971; O. Michikami et al., "Method of fabrication of Josephson tunnel junctions," U.S. Pat. 4,412,902, Nov. 1, 1983).~~ Control over oxide thickness and other properties in these studies were all the more remarkable in view of the fact that the oxides were typically grown on thick (e.g., 5,000 Å) metals such as Nb and Ta. In such metal-oxide systems, a range of layers and suboxides can also form, each having their own properties. In the present disclosure, control over the properties of the various TM oxides will be even better since very limited (perhaps 10 to 100 Å or so) thicknesses of metal are employed and thereby preclude the formation of significant quantities of unwanted, less controllable sub-oxide films. Thermodynamic forces will drive the oxide compositions to their most stable, fully oxidized state, e.g., Nb_2O_5, Ta_2O_5, etc. As noted above, it will still be necessary to crystallize these duplex oxide layers. Such treatments can be done by RTP and will be shorter than those used on MOCVD and sputter-deposited oxides since the stoichiometry and purity of the "low temperature oxides" need not be adjusted at high temperature.

The paragraph beginning at page 37, line 25 is amended as follows:

C29

Asymmetrical oxide tunnel barriers having a wide range of properties can also be grown via oxidation of alloy films of appropriate compositions ~~(see generally, J. Robertson and C.W. Chen, "Schottky barrier heights of tantalum oxide, barium strontium titanate, lead titanate, and strontium bismuth tantalate," Appl. Phys. Lett., vol. 74, no. 8, pp. 1168-1170, 22 Feb. 1999) and as referenced in the co-pending, co-filed application by L. Forbes and J.M. Eldridge, entitled "FLASH MEMORY DEVICES WITH METAL OXIDE INTERPLOY INSULATORS," attorney docket number 1303.014us1~~. Thin film barriers of platinum, palladium and similar noble metals must be added to prevent inter-diffusion and degradation of the perovskite oxides with the poly-Si layers. Some processing remarks are stated below.

The paragraph beginning at page 38, line 8 is amended as follows:

C30

For example, results have been obtained which demonstrate that at least a limited range of high temperature, super-conducting oxide films can be made by thermally oxidizing Y-Ba-Cu alloy films ~~(see generally, Hase et al., "Method of manufacturing an oxide superconducting film," U.S. Pat. 5,350,738, Sept. 27, 1994).~~ The present inventors have also disclosed how to employ "low temperature oxidation" and short thermal treatments in an inert ambient at 700 degrees Celsius in order to form a range of perovskite oxide films from parent alloy films ~~(see generally, J. M. Eldridge, "Low Cost Processes for Producing High Quality Perovskite Dielectric Films," application Serial No. _____).~~ The dielectric constants of crystallized, perovskite oxides can be very large, with values in the 100 to 1000 or more range. The basic process is more complicated than that needed to oxidize layered films of transition metals. (See Example II.) The TM layers would typically be pure metals although they could be alloyed. The TMs are similar metallurgically as are their oxides. In contrast, the parent alloy films that can be converted to a perovskite oxide are typically comprised of metals having widely different chemical reactivities with oxygen and other common gasses. In the Y-Ba-Cu system referenced above, Y and Ba are among the most reactive of metals while the reactivity of Cu approaches (albeit distantly) those of other noble metals. If the alloy is to be completely oxidized, then thin film barriers such as Pd, Pt, etc. or their conductive oxides must be added between the Si and the parent metal film to serve as: electrical contact layers; diffusion barriers; and, oxidation stops. In such a case, the Schottky barrier heights of various TM oxides and perovskite oxides in contact with various metals will help in the design of the tunnel device. In the more likely event that the perovskite parent alloy film will be only partially converted to oxide and then covered with a second layer of the parent alloy (recall the structure of Figure 2), then the barrier heights will represent that developed during oxide growth at the parent perovskite alloy/perovskite oxide interface. Obviously, such barrier heights cannot be predicted *ab initio* for such a wide class of materials but will have to be developed as the need arises. This information will have to be developed on a system-by-system basis.

The paragraph beginning at page 42, line 1 is amended as follows:

C31

Figure 11 [[14]] illustrates a block diagram of an embodiment of an electronic system 1101 ~~1401~~ according to the teachings of the present invention. In the embodiment shown in Figure 11 [[14]], the system 1101 ~~1401~~ includes a memory device 1100 ~~1400~~ which has an array of memory cells 1102 ~~1402~~, address decoder 1104 ~~1404~~, row access circuitry 1106 ~~1406~~, column access circuitry 1108 ~~1408~~, control circuitry 1110 ~~1410~~, and input/output circuit 1112 ~~1412~~. Also, as shown in Figure 11 [[14]], the circuit 1101 ~~1401~~ includes a processor 1114 ~~1414~~, or memory controller for memory accessing. The memory device 1100 ~~1400~~ receives control signals from the processor 1114 ~~1414~~, such as WE*, RAS* and CAS* signals over wiring or metallization lines. The memory device 1100 ~~1400~~ is used to store data which is accessed via I/O lines. It will be appreciated by those skilled in the art that additional circuitry and control signals can be provided, and that the memory device 1100 ~~1400~~ has been simplified to help focus on the invention. At least one of the processor 1114 ~~1414~~ or memory device 1100 ~~1400~~ has a memory cell formed according to the embodiments of the present invention. That is, at least one of the processor 1114 ~~1414~~ or memory device 1100 ~~1400~~ includes an asymmetrical low tunnel barrier interpoly insulator according to the teachings of the present invention.

The paragraph beginning at page 42, line 18 is amended as follows:

C32

It will be understood that the embodiment shown in Figure 11 [[14]] illustrates an embodiment for electronic system circuitry in which the novel memory cells of the present invention are used. The illustration of system 1101 ~~1401~~, as shown in Figure 11 [[14]], is intended to provide a general understanding of one application for the structure and circuitry of the present invention, and is not intended to serve as a complete description of all the elements and features of an electronic system using the novel memory cell structures. Further, the invention is equally applicable to any size and type of memory device 1100 ~~1400~~ using the novel memory cells of the present invention and is not intended to be limited to that described above. As one of ordinary skill in the art will understand, such an electronic system can be fabricated in single-package processing units, or even on a single semiconductor chip, in order to reduce the communication time between the processor and the memory device.